REMARKS

Applicants have noted the Office's entry of the request for continued examination under 37 C.F.R. §1.114. The previous arguments with respect to claims 7-12 and 14-15 have been considered but are not deemed persuasive.

Claims 7-12 and 14-15 are pending and have been rejected under 35 U.S.C. §103(a) as being assertedly unpatentable over Hirano et al. (USPN 6,445,011; "Hirano" hereinafter) in view of Tominaga (USPAP 2002/0008325; "Tominaga" hereinafter) and further in view of Okazaki et al. (USPN 5,298,768; "Okazaki" hereinafter).

Applicants have amended claim 7 according to FIG. 3 and paragraph [0023] of the specification of the present invention, so as to more clearly define the present invention over the cited art. Upon entry of the proposed amendments, Applicants hereby respectfully traverse the rejections for the reasons given below. Reconsideration of the pending claims 7-12 and 14-15 is most earnestly requested.

Claim Rejections under 35 U.S.C. §103

Claims 7-12 and 14-15 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Hirano in view of Tominaga and further in view of Okazaki.

In response thereto, Applicants have revised claim 7 as recited below,

"A light-emitting diode package structure, comprising:

a semiconductor sub-mount having a first surface with a cavity therein and comprising a first conductive type semiconductor substrate and a second conductive type region enclosed by the first conductive type semiconductor substrate;

a first patterned conductive-reflective film set up on a portion of the first surface, a first sidewall of the cavity and a bottom surface of the cavity, wherein **the first patterned conductive-reflective film contacts with the first sidewall of the cavity and a part of the first conductive type semiconductor substrate**;

a second patterned conductive-reflective film set up on a portion of the first surface, a second sidewall of the cavity and a bottom surface of the cavity, wherein the second patterned conductive-reflective film covers the second sidewall of the cavity;

an insulating layer only set up in-between the semiconductor sub-mount and the second patterned conductive-reflective film; and

a light-emitting diode chip set up inside the cavity of the semiconductor sub-mount, wherein the light-emitting diode has a first electrode and a second electrode electrically connected to the first patterned conductive-reflective film and the second patterned conductive-reflective film." **(Emphasis added)**

Referring to FIG. 11B and the description on column 11, lines 21-27 of Hirano's specification, the positive electrode 422, as purportedly reading on the first patterned conductive-reflective film 210 of the instant case, is formed on the insulation film 424 and electrically connected to the n-layer 443 (as purportedly equivalent to the semiconductor substrate of the

instant case) via the windows formed in the insulation film 424. Hence, **the positive electrode 422 taught by Hirano directly contacts with the insulation film 424 and is indirectly connected to the n-layer 443 via the windows formed in the insulation film 424.** Nevertheless, referring to FIG. 3 and the amended claim 7 of the present invention, the first patterned conductive-reflective film 210 "**contacts with the first sidewall 204a of the cavity 204 and a part of the first conductive type semiconductor substrate" but not contacts with the insulation layer 212** as depicted in FIG. 3 of the current case. The insulating layer 206 is "**only set up in-between the semiconductor sub-mount 200 and the second patterned conductive-reflective film 212**" as set forth in the currently amended claim 7, thus yielding clear differences in comparison with the teaching of Hirano.

Since Tominaga and Okazaki both fail to cure the aforesaid deficiency of Hirano in rejecting claim 7 of the instant application, claim 7 should be patentable over Hirano in view of Tominaga and Okazaki, for the cited references of record, either alone or in combination, fail to teach or suggest at least the features of "**the first patterned conductive-reflective film contacts with the first sidewall of the cavity and a part of the first conductive type semiconductor substrate**" and "**an insulating layer only set up in-between the semiconductor sub-mount and the second patterned conductive-reflective film**" recited in Applicants' claim 7, rendering claim 7 non-obvious over the prior art references and placing claim 7 at issue and claims 8-12 and 14-15 depending upon the allowable claim 7 all in proper condition for allowance. Reconsideration and withdrawal of the rejection and allowance of the present invention are respectfully requested.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 7-12 and 14-15 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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